9. The device of claim 8, further comprising a plurality of pad patterns, a pad pattern being on a respective contact plug, and wherein the pad patterns electrically connect the MTJ structures to the contact plugs.

10. A magnetoresistive random access memory device, comprising:

a lower structure having a flat first upper surface on a substrate;

a plurality of magnetic tunnel junction (MTJ) structures, each MTJ structure comprising a pillar shape on the lower structure;

a capping layer pattern on a sidewall of each of the MTJ structures and on the lower structure between the MTJ structures;

a filling layer pattern on the capping layer pattern, the filling layer filling gaps between the MTJ structures, and a top surface of the filling layer being substantially coplanar with top surfaces of the MTJ structures;

bit lines on the filling layer pattern and the MTJ structures, each of the bit lines contacting the top surfaces of the MTJ structures; and

an etch-stop layer on the filling layer pattern between the bit lines.

11. The device of claim 10, wherein the etch-stop layer has a flat upper surface.

12. The device of claim 10, wherein the etch-stop layer comprises silicon nitride, silicon oxynitride or aluminum oxide.

13. The device of claim 10, wherein the capping layer pattern comprises silicon nitride or silicon oxynitride.

14. The device of claim 10, wherein the magnetoresistive random access memory device is part of a smart phone comprising a touch-screen display.

15. A magnetoresistive random access memory device, comprising:

a first insulating interlayer on a first region and a second region of a substrate, the first insulating region comprising a flat first upper surface;

a pattern structure comprising magnetic tunnel junction (MTJ) structures and a filling layer pattern between the MTJ structures on the first insulating interlayer over the first region, the pattern structure comprising a flat second upper surface higher than the first upper surface, and the MTJ structures comprising a pillar shape;

bit lines on the pattern structure, and each of the bit lines contacting top surfaces of the MTJ structures;

an etch-stop layer on the pattern structure between the bit lines on the first region and the first upper surface of the first insulating interlayer on the second region, a first portion of an upper surface of the etch-stop layer on the first region being higher than a second portion of the upper surface of the etch-stop layer on the second region; and

a second insulating interlayer on the etch-stop layer on the first and second regions, the second insulating interlayer filling gaps between the bit lines.

16. The device of claim 15, further comprising a capping layer pattern on a sidewall of each of the MTJ structures and the first insulating interlayer between the MTJ structures on the first region.

17. The device of claim 16, wherein the capping layer pattern comprises silicon nitride or silicon oxynitride.

18. The device of claim 15, wherein the etch-stop layer is formed on the entire first upper surface of the first insulating interlayer on the second region, a sidewall of the filling layer at an interface between the first and second regions, and a portion of an upper surface of the filling layer, and

wherein the etch-stop layer comprises silicon nitride, silicon oxynitride or aluminum oxide.

19. The device of claim 10, wherein the magnetoresistive random access memory device is part of a smart phone comprising a touch-screen display.

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